IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jaroslav Hynecek	Art. Unit:	3663
Serial No.:	10/633,993	Examiner:	Johannes P. Mondt
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For: Clocked Barrier Virtual Phase FF, FT, and FIT CCD Image Sensors with Charge Multiplication Readout

APPELLANTS' AMENDED BRIEF UNDER 37 C.F.R. §1.192

Commissioner for Patents
P. Box. 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Amended Summary of Claimed Subject Matter in connection with the above-identified application in response to the Notification of Non-Compliant Appeal Brief #2 mailed January 8, 2008. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

SUMMARY OF CLAIMED SUBJECT MATTER

Specification page 10, line 23 to page 13, line 4, provides a concise explanation of the invention defined in independent claim 11.

The first clocked gate in claim 11 is gate electrode 307 in Figure 3 and gate electrode 409 in Figure 4.

The field plate in claim 11 is field plate gates 305 in Figure 3 and field plate gates 407 in Figure 4.

The second clocked gate in claim 11 is gate electrode 309 in Figure 3 and gate electrode 410 in Figure 4.

In FIG. 3, the first deposited layer of poly-silicon forms field plate gates 305 (field plate in claim 11), which are connected using metal wiring 306 to bias terminal. The second poly-silicon layer, separated form the first one by an oxide dielectric layer, forms separate and independently biased gate electrodes 307 (first clocked gate in claim 11) and 309 (second clocked gate in claim 11), which are also connected using respective metal wirings 308 and 310 to corresponding bias terminals. Directionality of charge transfer is established by placing suitable barrier implants 303 under a portion of each gate 307 (first clocked gate in claim 11) and 309 (second clocked gate in claim 11). The above described gate structure, after partial depletion of mobile charge, creates potential profile in each pixel that is described by segments 314, 315, 311, 312, and 313. In this example gate 307 (first clocked gate in claim 11) is biased in its high biasing level and gate 309 (second clocked gate in claim 11) in its low biasing level. Circles 317 indicate the electron charge transfer within the pixel. It is important to note that field plate gate 305 (field plate in claim 11) is biased at a DC biasing level and is not clocked. Introducing field plate into the gate structure has two advantages. The field plate is used to create a suitable potential profile that confines charge in the direction perpendicular to the plane of the drawing without the necessity for heavily doped p+ channel stops. This eliminates the source of unwanted clocking induced dark current caused by impact ionization within such channel stops. The second advantage is a better control of potential profile when this pixel structure is used in charge multiplying registers and the charge-multiplying gate needs to be biased to high biasing levels necessary for the onset of electron multiplication.

In Figure 4, gate 403 interfaces with virtual well region 402 and virtual barrier region 406 that further interfaces with field plate region 407 (field plate in claim 11) of the serial register. Field plate region 407 (field plate in claim 11), formed from the first poly-silicon layer, has openings 415 and notches 413 that are overlaid by the second poly-silicon layer, which forms gates 409 (first clocked gate in claim 11) and 410 (second clocked gate in claim 11). Metal wirings 408, 411, and 412 serve as interconnects between gates, the field plate, and the biasing terminals. Charge flow directionality is established by implanting barrier regions 414 and 416 under gates 409 (first clocked gate in claim 11) and 410 (second clocked gate in claim 11). Charge that is transferred from memory area into the serial register flows from Virtual Barrier region 406 under field plate region 422 and further under gate 409. Charge is confined to stay in these regions by suitable potential barrier forming implants 417 and 418 that have replaced the traditional p+ channel stops used in conventional designs. It is thus apparent that gates 409 and 410, which transport charge in serial register do not overlap any p+ channel stop anywhere.

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Respectfully submitted,

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